C SCI 113 INTRODUCTION TO COMPUTER ORGANIZATION
Spring 2002

MIDTERM EXAMINATION

Name: _____
I.D. No._____

March 5, 2002, 12:30 - 13:45
Total: **40 points**

Problem 1 (6 points)

(a) What is the **16-bit** number in two's complement representation equivalent to the decimal number A = +286 ? Write your result in **hexadecimal** notation.

(b) What is the **8-bit** number in two's complement representation equivalent to the decimal number B = -94 ? Write your result in **hexadecimal** notation.

(c) Perform the operation A+B manually as if you were performing the operation in a computer. Give the result of the sum and statuses N, V, Z, and C. You may write in **hexadecimal** notation.

(d) Perform the operation A-B manually as if you were performing the operation in a computer. Give the result of the difference and statuses N, V, Z, and C. You may write in **hexadecimal** notation.

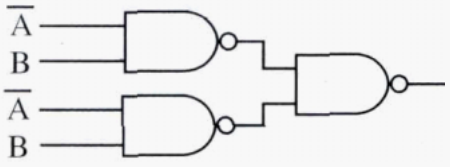
Problem 2 (3 points)

Remove the inverted signs from the input variables in each of the following circuits, but not increasing the number of gates. You should decrease the number of gates whenever possible. **Don't use the gates with inverted inputs.**

Give necessary explanation of your answer, either algebraically or graphically.

(a)

(b)



(c)

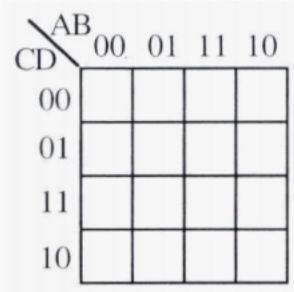
Problem 3 (4 points)

Given the function

$$F(A,B,C,D) = \sum (m0, m2, m3, m5, m6, m8, m9)$$

with 4 input variables, A, B, C, and D, where ABCD is the BCD code of a decimal digit. For maximum simplification of the function F, **all the invalid BCD codes above 1001 must be used as "don't care" conditions**.

(a) Draw the Karnaugh map for F.



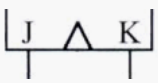
(b) Use the Karnaugh map to derive the simplest SOP expression for F.

(c) Use Boolean algebra to further simplify the above-obtained SOP expression for an **optimum implementation,** i.e., transform the expression into a form such that a minimum number of only 2-input basic gates selected from AND, OR, NAND, NOR, XOR, and XNOR can be used. The inverted variables, $\overline{A}$, $\overline{B}$, $\overline{C}$, and $\overline{D}$, are given.

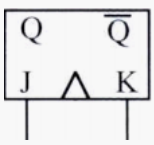
Problem 5 (3 points)

There are four types of flip-flops, SR, JK, T, and D. Look at the following three cases to show that they are interchangeable.

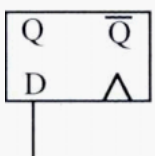
(a) Given a JK flip-flop below, how can you connect its J and K inputs through some gate(s) into an input D so that the JK flip-flop can work as a D flip-flop? Give your explanation and complete the circuit diagram.



(b) Given a JK flip-flop below, how can you connect its J and K inputs into an input T so that the JK flip-flop can work as a T flip-flop? Give your explanation and complete the circuit diagram.

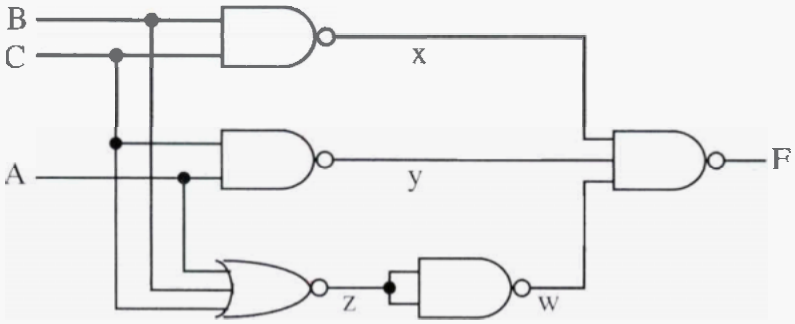


(c) Given a D flip-flop below, how can you connect its D input with some gate(s) into an input T so that the D flip-flop can work as a T flip-flop? Give your explanation and complete the circuit diagram.



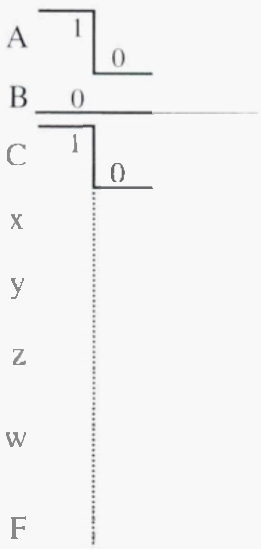
Problem 4 (12 points)

Given a combinational circuit below.



(a) Analyze the circuit to show that F has a hazard during the transition ABC = 101 → 000.
Note: Show your analysis within the circuit diagram.

(b) Assuming one unit of delay for every gate in the circuit, draw the waveform diagram for A, B, C, x, y, z, w, and F for the above transition and find the delay of F in number of unit gate delays.

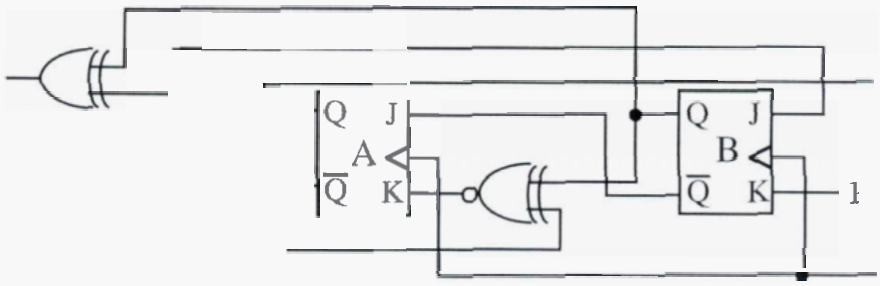


Delay of output F = _____ gate delays

(c) Using Boolean algebra, derive the logical expression for F in SOP form, and then simplify the SOP expression so that it can be implemented by only **two 2-input basic gates** selected from AND, OR, NAND, NOR, XOR, and XNOR. Input variables $\overline{A}$, $\overline{B}$, and $\overline{C}$ **are not available.**

Problem 6 (12 points)

Given a sequential circuit below



(b) Derive the state-transition table and output table.

(c) Draw the state-transition diagram. Find the counting sequences for x=0 and x=1. Is the circuit self-correcting, i.e., can any state that is not in the counting sequence be converged into the counting sequence?

(d) Draw the waveform diagram for A, B, and F with the input waveforms given in the figure. Assume positive edge-triggered flip-flops and the initial state of AB = 10 to start simulation. Neglect the delay of fl'p-flops and gates.