C SCI 113 INTRODUCTION TO COMPUTER ORGANIZATION

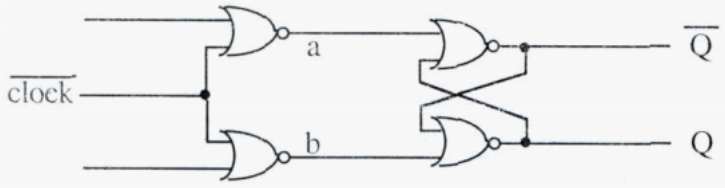
Midterm Examination 2

Name: _____ ____ ____ _____

I.D. No. _____ _____ Total: 20 points

Problem 1 (6 points)

Given the conceptual circuit of the NOR-based level-controlled clocked SR flip-flop as shown below.



(a) Trace the circuit to determine its state-transition table. Only when you trace the circuit, you can correctly determine which input should be *set*, which input should be *reset*, and what are the correct polarities (original or inverted) of them. As a hint to this problem, the outputs and the clock input are already named for you. You should give correct names to the inputs according to their functions and polarities. Then derive the state transition table and the state-transition diagram.

(b) To verify your state-transition table, trace the circuit gate by gate for the following two cases. You must give the changes of states at all the points including points 'a' and 'b' in the circuit, and then draw the waveform diagram to show the delays for all the points in the order of tracing.

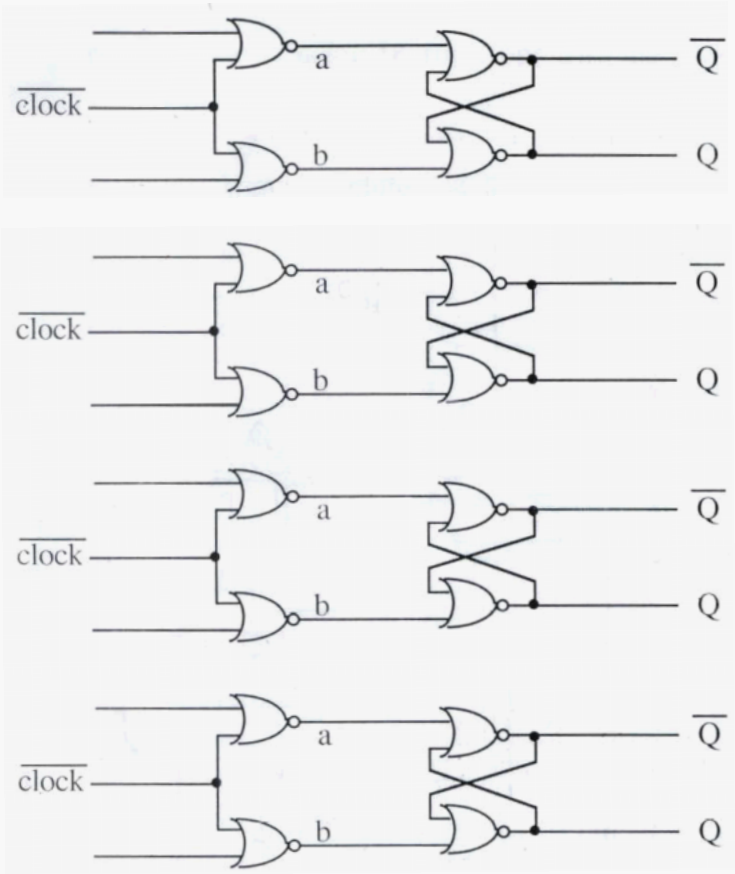
Case 1:

(i) When S = 0, R = 1, Q = 1, and $\overline{\text{clock}}$ = 1, show that the flip-flop can be in a stable state.

(ii) Then $\overline{\text{clock}}$ = 1 → 0, how does the circuit work and change its state?

(iii) While $\overline{\text{clock}}$ keeps '0' and S = 0 → 1, R = 1 → 0, how does the circuit respond?

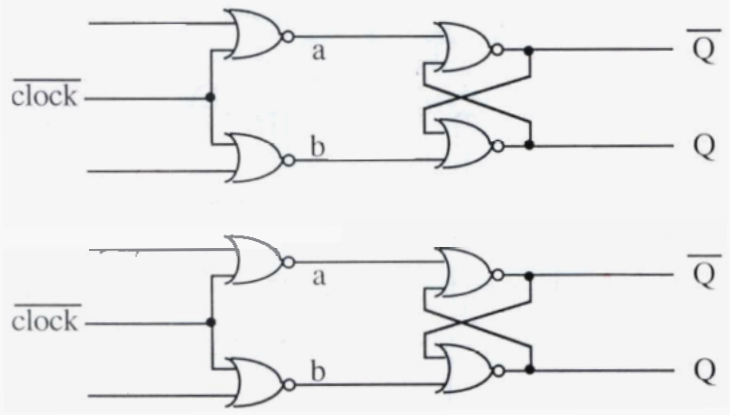
(iv) Then $\overline{\text{clock}}$ returns to '1', how does the circuit respond?



Case 2:

Repeat Case 1 (i), (ii) and (iv) for the initial state when S = 1, R = 1, Q = 1, and $\overline{\text{clock}}$ = 1.

Q



Problem 2 (7 points)

(a) Design a counter using JK flip-flops with the reversed "*add 3 mod 8*" counting sequence as given below:

$$000 \rightarrow 101 \rightarrow 010 \rightarrow 111 \rightarrow 100 \rightarrow 001 \rightarrow 110 \rightarrow 011 \rightarrow 000 \text{ (repeat)}$$

Give the detailed design procedure and derive the simplest expressions for the excitation signals.

Note: Circuit diagram is not required. It should be part of the final circuit to be drawn in Part (b)

(b) Include two control signals s_1s_0 into the circuit with the following function table:

Function select s_1	s_0	Functions	Explanation
0	0	maintain	no change
0	1	reset	reset to 000
1	0	reversed "add 1 mod 8" counting	Ordinary 3-bit binary down-counting
1	1	reversed "add 3 mod 8" counting	Counting in the above given sequence

Give the design procedure. Derive the simplest expressions and draw the circuit diagram.

Notes: (1) You must optimize your design by using a minimum number of gates (AND, OR, NOT, NAND, NOR, XOR, and XNOR) in implementaion. (2) You must reset the counter by $s_1s_0 = 01$, not using the Reset and Preset inputs of the flip-flops.

Problem 3 (7 points)

Design a 4-bit ALU on four full adders using their internal gates to implement the logical operations. The function table of the ALU is given below:

Function code s_2	s_1	s_0	Operation	Output F
0	0	0	add	OP1 plus OP2
0	0	1	subtract	OP1 minus OP2
0	1	0	reverse sub	OP2 minus OP1
0	1	1	decrement	OP1 minus 1
1	0	0	OR	$OP1_i \vee OP2_i$
1	0	1	XOR	$OP1_i \oplus OP2_i$
1	1	0	AND	$OP1_i \wedge OP2_i$
1	1	1	XNOR	$\overline{OP1_i \oplus OP2_i}$

Give the detailed design procedure including:

(a) Write the truth table for the input variables A_i, B_i, C_{i-1} of the full adder and the output of the ALU.

(b) Draw the Karnaugh maps for these variables.

(c) Derive the simplest expressions for these variables so that the total number of gates (AND, OR, NOT, NAND, NOR, XOR, and XNOR) to be used will be minimum.

(d) Draw the circuit diagram of the ALU. You may draw only for the i-th bit of the ALU, $0 \le i \le 3$, using the XOR-based full-adder circuit, plus a circuit for the C_{-1}. The circuits for the status bits are not required.